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Information Disclosure Statement By Applicant	Applicant: Esposito et al.	
(Use Several Sheets if Necessary)	Filing Date March 18, 2004	Group 2631

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
/MY/	A	6,401,230	06/04/02	Ahanessians et al.			02/01/99
/MY/	B	6,600,788	07/29/03	Dick, et al.			09/10/99
	C						
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	E						

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
/MY/	O	San et al., "Finite Impulse Response (Fir) Filter Compiler," U.S. Patent Application No. 09/773,853, filed January 31, 2001
/MY/	P	D'souza Et Al., "Dynamically Re-Configurable Signal Decimation System Using A Finite Impulse Response (Fir) Filter," U.S. Patent Application No. 10/396,194, filed March 24, 2003
/MY/	Q	Shung et al., "An integrated CAD system for Algorithm-Specific IC Design", IEEE Transactions on Computer-Aided Design, Vol. 10, No. 4, April 1991
/MY/	R	Saramaki et al., "Digital Filtering in FPGAs", 1994 Conference Record of the Twenty-eighth Asilomar Conference on Signals, Systems, and Computers, Vol. 2, pp. 1373-1377, 1994
/MY/	S	Jain et al., "FIRGEN: A computer-aided design System for High Performance FIR Filter Integrated Circuits", IEEE Transactions on Signal Processing, Vol. 39, No. 7, July 1991
/MY/	T	San et al., "Finite Impulse Response (Fir) Filter Compiler," U.S. Patent Application No. 09/773,853, filed January 31, 2001, Office Action Mailed July 15, 2004
/MY/	U	San et al., "Finite Impulse Response (Fir) Filter Compiler," U.S. Patent Application No. 09/773,853, filed January 31, 2001, Final Office Action Mailed December 17, 2004
Examiner	/Michael Yaary/	Date Considered 07/27/2007

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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